S/N 09/800,703

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Dustin P. Wood	Examiner:	David Graybill
Serial No.:	09/800,703	Group Art Unit:	2827
Filed:	March 7, 2001	Docket No.:	884.159US2
Title:	CHIP PACKAGE WITH DEGASSING HOLES		
Assignee:	Intel Corporation	Customer No.	21186

**APPEAL BRIEF TO THE BOARD OF
PATENT APPEALS AND INTERFERENCES OF THE
UNITED STATES PATENT AND TRADEMARK OFFICE**

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Appellant's Brief on Appeal

This brief is presented in Appeal from the final rejection of claims 30, 35, and 37 of the above identified application. The Final Office Action from which the Appellant hereby appeals was mailed on December 15, 2003.

The appeal brief is filed in triplicate. Please charge the requisite fee of \$330 as set forth in 37 C.F.R. § 1.17(f) to Deposit Account 19-0743. Appellant respectfully requests reversal of the Examiner's rejection of pending claims 30, 35, and 37. Appellant reserves the right to request an Oral Hearing at a later date.

1. Real Party in Interest

The real party in interest of the above-captioned patent application is the assignee, Intel Corporation, a corporation organized and existing under and by virtue of the laws of the State of Delaware, and having an office and place of business at 2200 Mission College Blvd., Santa Clara, California, 95052.

2. Related Appeals and Interferences

There are no other appeals or interferences known to the Appellant which will have a bearing on the Board's decision in the present appeal.

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3. Status of the Claims

Claims 30, 35, and 37 are pending in the present application, and stand under Final Rejection. Claim 35 was objected to under 35 U.S.C. §112, first paragraph, and rejected under 35 U.S.C. §102(b). Claim 30 was similarly rejected under 35 U.S.C. §102(b), and claim 37 was rejected under 35 USC § 103(a). These three claims are the subject of the present appeal.

4. Status of Amendments

The claims presented here for consideration are not amended, and no amendments are pending.

5. Summary of the Invention

In one example embodiment of the invention, a semiconductor device package includes multiple built-up layers of metal sandwiching non-conductive layers. The metal layers have grids of degassing holes arranged in rows and columns. The rows and columns are locatable via a first coordinate system. Signal traces are embedded within the non-conductive layers such that the signal traces are also sandwiched between the metal layers with degassing holes. The signal traces generally run at zero degrees, 45 degrees, and 90 degrees relative to a second coordinate system. The first coordinate system is rotated relative to the second coordinate system to lower impedance variations of different traces. Impedance variations decrease due to the decreased variation in the number of degassing holes passed over or under by a trace. The grid of degassing holes on one metal layer can be offset in two dimensions relative to the degassing holes on another layer.

6. Issues Presented for Review

1. Whether claim 35 is unpatentable under 35 USC § 112, first paragraph.
2. Whether claims 30 and 35 are unpatentable under 35 USC § 102(b) over Duxbury (U.S. 5,360,949).

3. Whether claim 37 is unpatentable under 35 USC § 103(a) over Duxbury in view of Tanahashi (U.S. 6,184,477).

7. Grouping of Claims

Applicant believes that claim 30 and its dependent claim 37 should be considered together as a group, but elects to further address claim 35 separately. Although claim 35 depends from independent claim 30, it is rejected under §112 grounds not applied to claim 30, which are independently addressed herein.

8. Argument

1) The Applicable Law

To sustain a rejection under 35 U.S.C. §102(b) or §103(a), the reference (or references when combined) must teach or suggest all the claim elements. M.P.E.P. § 2142 (citing *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed.Cir. 1991)). The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991); MPEP § 2143. The Examiner must avoid hindsight. *In re Bond*, 910 F.2d 831, 834, 15 USPQ2d 1566, 1568 (Fed. Cir. 1990).

Further, the fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990); MPEP § 2143.01. The prior art must provide a motivation or reasons for the worker in the art, without the benefit of the specification, to make the necessary changes in the reference device. *Ex parte Chicago Rawhide MFG. Co.*, 223 USPQ 351, 353 (Bd. Pat. Ap. & Inter. 1984). MPEP § 2144.05(VI)B.

2) Discussion of the Rejections

1. Whether claim 35 is unpatentable under 35 USC § 112, first paragraph.

The Office Action suggests that the application fails to describe in the specification the claim limitation “the at least one conductive signal trace includes at least one segment rotated”, such that it would reasonably convey to one skilled in the art that applicant had possession of the claimed invention at the time of filing.

Applicant respectfully points out that support for this language has been shown to be present in the specification. More specifically, page 10 describes (referring to Figure 6) in the paragraph from line 15-24 how signal traces run at various angles depending in part on selection of angle 610.

More generally, the text of p. 9, ln. 12 through p. 10, ln. 23, discusses how traces are rotated based in part on configuration of degassing holes shown in Figure 6, and in part based on impedance variation. The axes about which the traces are rotated is described and illustrated, such as with respect to angle 610 in Figure 6.

Because the specification describes in detail how the traces are rotated, and gives examples accompanied by illustrations, applicant believes claim 35 is in condition for allowance, and respectfully requests reversal of the rejection of this claim.

2. Whether claims 30 and 35 are unpatentable under 35 USC § 102(b) over Duxbury (U.S. 5,360,949).

Duxbury describes a printed circuit board in which pairs of conductive wires are supported by a flexible nonconductive sheet which is placed between two conductive ground meshes. The angle that the conductive wire traces take relative to the orientation of the conductive mesh is selected to vary the offset of mesh interconnection points from the conductive wires. The application further discusses that it may be adapted to a multilayer printed circuit board, and that the ground mesh may be replaced with a plurality of holes in the form of a matrix.

Duxbury first fails to consider an integrated circuit package, as is the subject of the present claims here rejected.

Duxbury also does not teach offsetting a second conductive layer having a second grid of holes from a first conductive layer having a first grid of holes. The description of Duxbury's Figure 4 clearly recites that "the upper mesh conductors 36 are parallel to the lower mesh conductors 38" (*see*, col. 4, ln. 36-37). Duxbury therefore does not teach offsetting first and second conductive layers having grids of holes offset with respect to one another.

Duxbury does recite that a mesh may in another embodiment be a conductive sheet with a plurality of holes as shown in Figure 7, but these holes are simply holes in a conductive mesh through which vias may be routed. As previously discussed, Duxbury also fails to consider a second mesh having holes offset with respect to the first mesh.

Duxbury also fails to consider disposing its various elements in accordance with the relative coordinate systems present in claim 30 and its dependent claim 35.

Because Duxbury fails to teach an integrated circuit package, fails to teach offsetting first and second conductive layers having grids of holes offset with respect to one another, and fails to teach at least one further conductive signal trace rotated with respect to the holes of the first conductive layer's hole axis, applicant believes the claims as amended are in condition for allowance. Applicant therefore respectfully requests reversal of the rejection of claim 30, and of claims 35 and 37 which depend therefrom.

3. *Whether claim 37 is unpatentable under 35 USC § 103(a) over Duxbury in view of Tanahashi (U.S. 6,184,477).*

Applicant believes that the discussion presented above is further applicable here, and incorporates the above discussion by reference. Because this claim depends from base claim 30 believed to be in condition for allowance as described above, it is believed to be allowable as based on an allowable base claim, and is grouped for purposes of this appeal with Claim 30. For these reasons, reversal of the rejection of claim 37 is respectfully requested.

9. Conclusion

Applicant believes the claims are in condition for allowance, and request withdrawal of the rejections to the pending claims. It is respectfully submitted that the cited art fails to anticipate the present invention or to render it obvious, and that the claimed invention is therefore patentably distinct from the cited art. It is respectfully submitted that claims 30, 35, and 37 should therefore be allowed, and reversal of the Examiner's rejections of pending claims 30, 35, and 37 is respectfully requested.

Respectfully submitted,

Dustin P. Wood

By his representatives,

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Date

May 17 04

By



John M. Dahl

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Name

KACIA LEE

Signature

Kacia Lee

Appendix A: Pending Claims

1-29. (Cancelled)

30. (Previously Presented) An integrated circuit package comprising:
a first conductive layer having a first grid of holes disposed relative to a first coordinate system;
a second conductive layer parallel to the first conductive layer, the second conductive layer having a second grid of holes offset from the first grid of holes and disposed relative to the first coordinate system;
a dielectric layer between the first and second conductive layers; and
at least one conductive signal trace disposed within the dielectric layer, the at least one conductive signal trace disposed parallel to an axis of a second coordinate system that is rotated with respect to the first coordinate system by an angle of between zero and forty-five degrees.

31. (Cancelled) The integrated circuit package of claim 30 further comprising a signal layer embedded in the dielectric layer.

32. (Cancelled) The integrated circuit package of claim 31 wherein the signal layer includes at least one signal trace.

33. (Cancelled)

34. (Cancelled) The integrated circuit package of claim 32 wherein the first and second grids of holes have an x direction and a y direction, neither of which being parallel to the at least one signal trace.

APPLICANT'S BRIEF ON APPEAL

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35. (Previously Presented) The integrated circuit package of claim 34 wherein the at least one conductive signal trace includes at least one segment rotated substantially 22.5 degrees relative to the first coordinate system.

36. (Cancelled)

37. (Previously Presented) The integrated circuit package of claim 30 wherein the first grid of holes includes holes spaced with non-equal pitch in an x direction and in a y direction relative to the first coordinate system.

38-54. (Cancelled)

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AF/2822#
IFW

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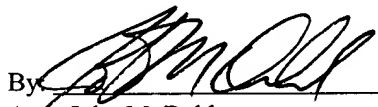
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We are transmitting herewith the following attached items (as indicated with an "X"):

- ☒ A return postcard.
- ☒ Appeal Brief (8 Pages) in triplicate.
- ☒ Authorization to charge Deposit Account 19-0743 in the amount of \$330.00 for submission of a brief in support of an appeal.

If not provided for in a separate paper filed herewith, Please consider this a PETITION FOR EXTENSION OF TIME for sufficient number of months to enter these papers and please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
Customer Number 21186

By 
Atty: John M. Dahl
Reg. No. 44,639

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KACIA LEE
Name

Kacia Lee
Signature

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
(GENERAL)